Pulse and ESD
Technology

1024 pins ESD/Latch-up Tester

Model 7000-1024

Specification and Technical Information

Tokyo Electronics Trading Co., Ltd
8-26, 4 Chome, Nishiki-cho, Tachikawa-shi
Tokyo 190-0022 Japan
Tel:+81-42-548-8011
Fax:+81-42-548-8013
URL : www.tet.co.jp

1. Specifications

1.1 ESD Simulation

- Pin Selection Method
  E & EL type : Automatic by 2 axes robot
  L type : Manual
- High Voltage
  E & EL type : ±1000/4500/(8000)V, 1%±5V
  L type : ±1000V, 1%±5V
- CR Unit : HBM, MM and others
- ESD Repetition : 1 ~100 times
- ESD Period : 300ms ~ 5s, 100ms increment
- Charge removal : 3 ways selected by program

1.2 DC measurement

- V_{cc1} Power Supply(Used as pulsed power supply, as well)
  Voltage Range : ±30V, 50mV increments
  Current Measurement :
  ESD Test : ±500mA, 100nA(Min.) resolution
  Latch-up Test : ±1000mA, 1mA(Min.) resolution
  Current Limiter : 50mA ~ 1000mA, 10mA increments
  Pulse Width : 0.1ms ~ 5s
  T_r, T_f : 3μs/V
  Latch-up definition current : I_{CCQ} × N + Offset
  I_{CCQ} : Quiescent current
  N : 1 ~100
  Offset: 5mA ~ 1000mA, 5mA increments
  DUT connection : Automated
- $V_{cc2\sim4}$(DC Power Supply)
  Voltage Range : ±15V, 50mV increments
  Current Measurement : Same as V_{cc1}
  Current Limiter : Same as V_{cc1}
  Latch-up definition current : Same as V_{cc1}
  DUT connection : Automated
- VF/IM(Voltage Force/Current Measurement)
  Voltage Range : ±15V, 10mV increments
  Current Measurement : 100mA, 10nA(Min.) resolution
  Current Range : 5 Auto-ranges
  Averaging : 1, 2, 4, 8, 16, 32 times
  DUT Connection : Automated
- DVM(Digital Voltmeter)
  Voltage Measurement : ±30V, 10mV (Min.) resolution
  Input impedance : Over 10MΩ
  DUT Connection : Automated

1.3 Latch-up Trigger Source

- i_p(Current Pulse) Generator
  Current Range : ±1000mA, 1mA(Min.) increments
  Voltage Measurement : ±30V, 50mV resolution
  Clamp Voltage : 1 ~ 30V, 0.1V increments
  Pulse Width : 0.1ms ~ 1s, 0.1ms increments
  T_r, T_f : about 10μs/200mA
  Repetition : 1 ~ 100 times
  Period : 100ms ~ 10s, 100ms increment
  DUT Connection : Automated
- v_p(Voltage Pulse) Generator
  Voltage Range : ±30V, 50mV increments
  Current Measurement : ±1000mA, 1mA(Min.) resolution
  Current Limiter : 50mA ~ 1000mA, 10mA increments
  Pulse Width : 0.2ms ~ 5s, 0.2ms increments
  T_r, T_f : about 50μs/10V
  Repetition : 1 ~ 100 times
  Period : 100ms ~ 10s, 100ms increment
  DUT Connection : Automated

1.4 DUT Stabilization

- Pull-up/down
  Connected to $V_{cc1\sim4}$, GND, VUD1~VUD3 or maxLogicHi/minLogicLo via 10kΩ.
  DUT Connection : Automated
- Multi-channel Control Power Supply
  Channels : 4
  Voltage Range : ±30V, Potentiometer control
  Voltage Display : 3.5 digits LED with polarity
  Current : 10mA
  Current Measurement : 3.5 digits LED with polarity
- 4 Channels Clock Generator
  Period, Frequency:
  CH1 : 10k, 100k, 1MHz selectable
  CH2 : Invert of CH1
  CH3 : 1μs ~ 100 μs, 1μs increments
  CH4 : 1μs ~ 100 μs, 1μs increments
  Output Level : 1V ~ 15V, 0.1V increments
  DUT Connection : Manually by jumper leads
- 16 Channels Pattern Generator
  Channels : 1 Clock Channel
  16 Pattern Channels

Clock : 1μs ~ 100 μs, 1μs increments or 100Mz (optional)
Pattern Timing : Clock Synchronous
Pattern Depth : 1024 vectors
Pattern Group : 2(A and B)
Output Pattern :Only B or B × n after A
Output Level : 1V ~ 15V, 0.1V increments
DUT Connection : Manually by jumper leads

1.5 Other Options
Temperature controlled Oven : Room temp., +25° ~ 125°C
Emission Microscope
Digital Oscilloscope

1.6 Dimension, Power Requirement
Main Body Size : Approx. 1100(W), 900(H), 800(D) mm
Main Body Weight : Less than 200kg
AC Supply : 100V ±10%, 50/60Hz, Single Phase 1.5kVA(MAX.)
Ambient Temperature : +10° ~ 40°C
(note) : Other AC supply voltage may be ordered as an option.

2. Features

- **Up to 1024 pins with full pin combination capability**
- **Allows ESD(HBM and MM) and Latch-up Tests**
- **Meets JEDEC, MIL, ESD Association and EIAJ standards, as well as future standards**
- **Drastic Test Time Reduction**
- **True constant current pulse and fast pulsed power supply**
- **Stabilizes DUT by pull-up/down and pattern generator**
- **Collects detail test results quickly by auto or manual operation**
- **Allows temperature coefficient test**
- **Minimum path resistance of power supplies**
- **Damage detection between tests**
- **Discharge between zap(s)**
- **Tests multiple DUT, multiple supply DUT and LCD drivers**
- **Function test available**
- **Low insertion force connectors on DUT board**
- **Complete diagnostics and easy maintenance**
- **Connectable with Ethernet**
- **Allows data manipulation by the data base program**

3. General

Higher integration and higher speed are increasingly developed day by day in the semiconductor market. It is especially drastic in memory, microprocessor, ASIC and LCD driver. Therefore, the reliability evaluation against ESD(Electro-Static Discharge) and Latch-up of these semiconductor devices is becoming more important. Model 7000 series targets all of these tests by a single system. It allows latch-up test of CMOS LSI with multiple power supply.

The Model 7000 series is a states of the arts reliability evaluation system that allows fully automated ESD test and Latch-up test up to 1024 pin devices. 3 types are available for the series.

Type E : ESD test only
Type L : Latch-up test only
Type EL : Both ESD and Latch-up test

- **ESD test**

ESD Pulse Generator (EPG) unit is attached to a 2 axes robot. The ESD pulse generated in the unit zaps DUT and returns to the unit with the minimum path length so that HBM, MM or other waveform specification may be installed. Each EPG unit includes 4 C/R and the system may have up to 4 robots (256 pins/robot). This means high speed zapping (more than 10 times faster than the predecessor) is available, maintaining zapping period to the same pin enough long as specified by the standard.

Though the Model 7000 adopts robots to define zapped pin, the return or common pin can be programmed

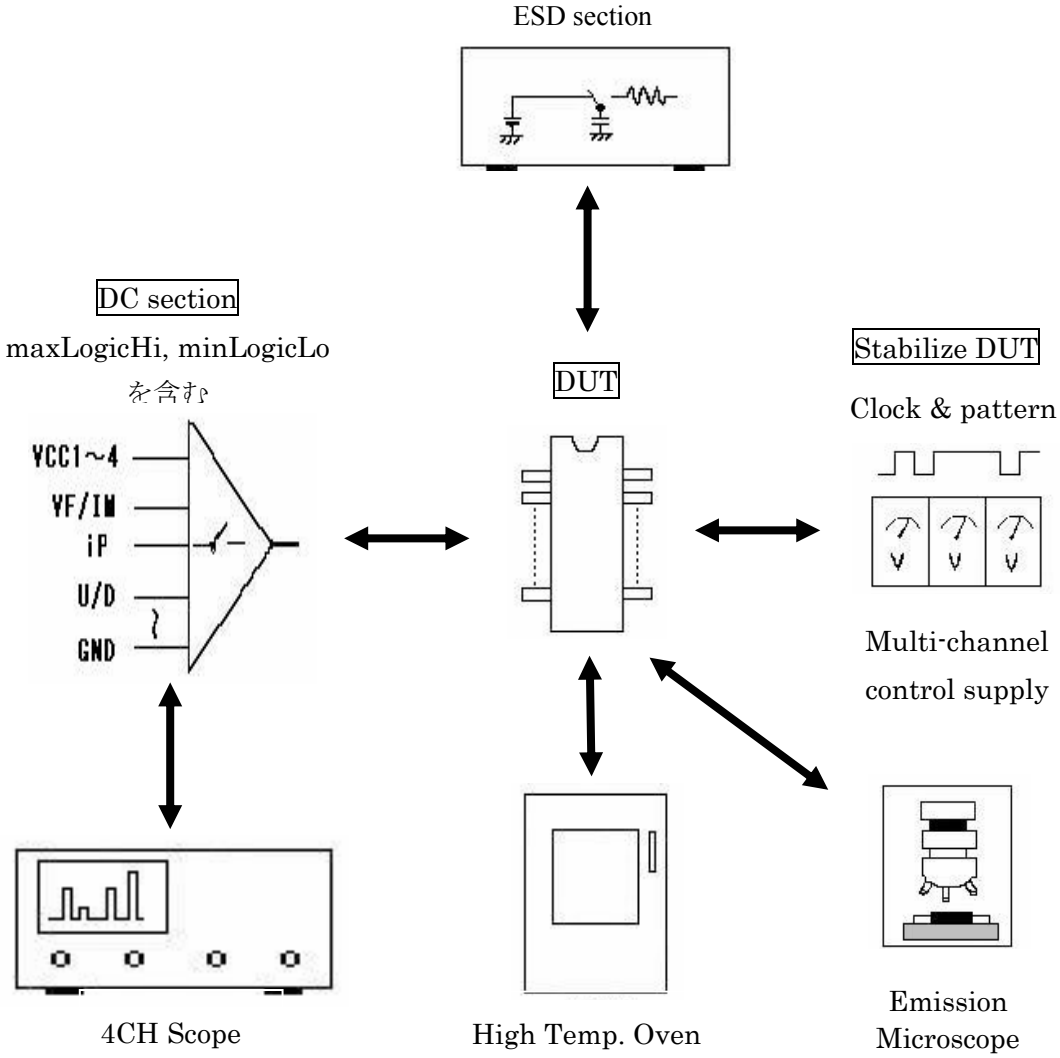
because relay matrix is installed for it. This allows full pin combination ESD test requested by the standards.
Degradation or breakage is detected by the measurement function included in the DC section.

- V-I curve variation(% method) before and after zapping
- against DC specification (M/M method) after zapping
- V-I curve is available for every pin and ESD voltage

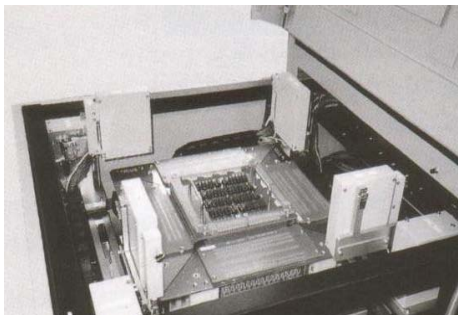
- Latch-up test

For latch-up test using trigger source such as current pulse (i_p), voltage pulse (v_p) or supply pulse (V_p), only DC section is used. For latch-up test using trigger source such as ESD pulse or transient pulse, ESD section is used as well.
Except the V_p latch-up test, high speed successive approximation procedures are available, to reduce test time.
Because latch-up detection is done by comparison between the quiescent I_{cc}(I_{ccq}) and I_{cc} after the trigger or by the absolute value of I_{cc} after the trigger, it is important to stabilize the DUT. For this purpose, Model 7000 allows to pull-up or pull-down every input pin, or supply clock or digital pattern by the stabilization section.
High temperature oven enables temperature coefficient measurement of latch-up.
Digitizing oscilloscope will give the waveform information how latch-up proceed.
Emission microscope gives visual data and hard copy of on-chip heat generation because of latch-up.

Block Diagram



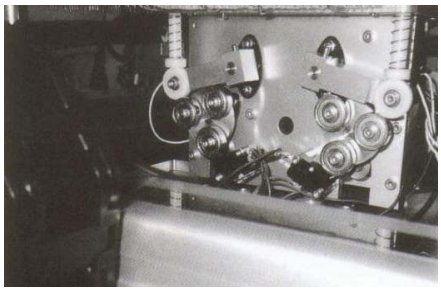
Position Control by miniature linear guide



Up to 4 EPG(ESD Pulse Generator) units can be flexibly controlled. Time spent for zapping is reduced down to less than 1/10 of predecessor.

- High speed zapping
- Double buffer mechanism
- 4 generators/unit
- 4 units/system

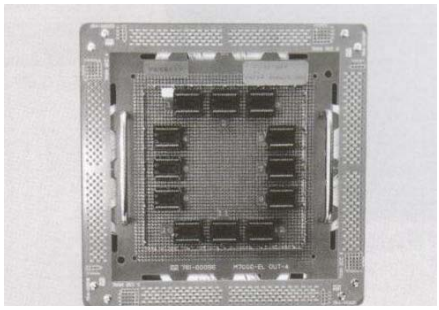
DUT Ejection Mechanism



Easy ejection of 512 pins DUT board

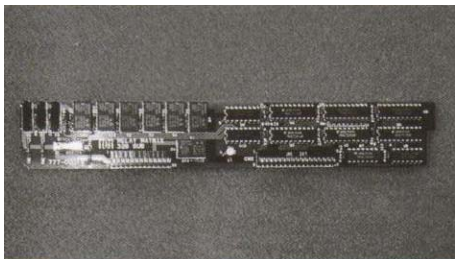
- Miss-feed Protection
- 2 sec to eject
- 60kg of ejection force
- Parallel feed/eject

Multiple Devices DUT Board



- Space grade connectors adopted
- High reliability, low contact resistance and low insertion force
- Can be used in the oven
- Can be used for both ESD and Latch-up test
- Common pin connection is done automatically or manually
- High Speed ESD mode available
- HBM/MM Mixed zapping to multiple DUT

Pin Electronics



One small PC board per pin

- Reliable 3A relay for V_{cc} and GND
- Very small relay for pull-up/down
- Low impedance path
- Easy maintenance

4. ESD Test (Model 7000E, EL type)

4.1 General

It was a common understanding that ESD test took long time. Model 7000 challenged the wall, and this is it. Multiple robot and multiple ESD generator in the unit enabled reduction of total time spent for zapping down to less than 1/10 compared to the predecessors.

ESD test standard have been up-graded every 2 or 3 years including waveform and pin combination specifications. Because Model 7000 adopted C/R unit to specify ESD waveform, most future waveform can be generated by modifying the C/R unit.

DC section is redesigned to improve the precision and speed.

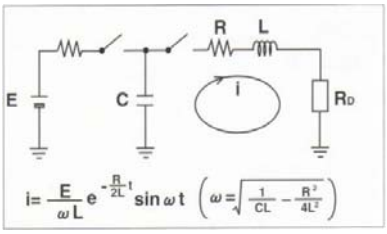
4.2 Features

- Meets EIAJ, MIL, ESD and JEDEC standards
- High speed zapping and DC measurement
- Programmable common(return) pins
- 3 discharge methods
- Up to 8kV ESD voltage (Less than 512 pins)
- Easy replacement of C/R units
- High speed and high precision DC measurement
- Flexible test procedure

4.3 Any ESD Waveform

By developing a C/R unit, any ESD waveform may be generated by the Model 7000 so that a variety of field failure modes may be simulated, especially in Machine Model.

- **Basic circuit**



E : High Voltage

C : Capacitance

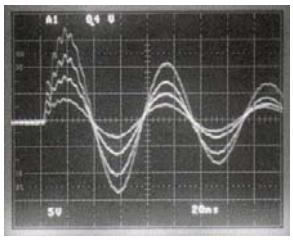
R : Discharge resistance

L : Discharge inductance

R_D: DUT resistance(0 Ω)

By deciding the L,C,R values, any waveform may be generated, and any failure mode is simulated.

A. ESD and JEDEC waveform and linearity

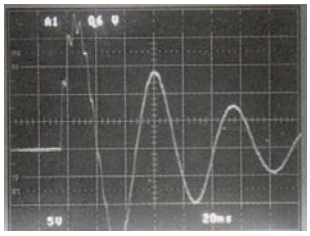


C=200pF, L=0.75μH, R=10Ω

E(V)	ips(A)	tm(ns)
200	3.4	76
400	6.5	76
600	10	76
800	13	76

Failure of oxide and junction are mainly simulated.

B. High stress waveform(customer dependent)

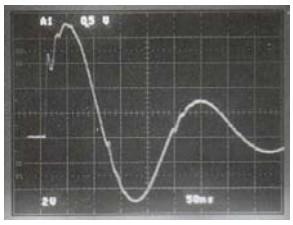


C=200pF, L=0.3μH, R=10Ω

E(V)	ips(A)	tm(ns)
400	10	54

Oxide failure is mainly simulated.

C. Thermal stress waveform(customer dependent)



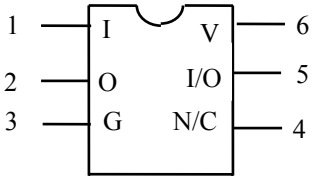
C=200pF, L=7μH, R=30Ω

E(V)	ips(A)	tm(ns)
400	1.8	760

Junction failure is mainly simulated.

4.4 Pin combination test

Common pins can be programmed as TET predecessors. In this method, common pins are automatically changed in sequence. To activate common pin, just enter check (V) in the selection column.



I : Input NC : No Connection
O : Output V : Supply Pin
I/O : Input/Output G : Ground Pin

Zap sequence	Zap pin	Common pin	Selection	Description
1	1	3	V	Zapped between signal pin, supply pin and ground (common) pin
2	2			
3	5			
4	6			
5	1	6		Zapped between signal pin, ground pin and supply pin
6	2			
7	3			
8	5			
9	1	2,5	V	Zapped between signal pin and signal pin
10	2	5,1		
11	5	1,2		

4.5 3 modes of DUT discharge

It was found that semiconductor device's endurance against ESD depends on DUT discharge method during zapping process. To make clear the dependence, Model 7000 allows 3 modes of discharge. ESD timings are kept as programmed.

Mode 1: Discharge is performed when zapping all selected pins or pin combinations are done.

Mode 2: Discharge is performed when zapping each pin or pin combination is done.

Mode 3: Discharge is performed after every zapping. If 3 zapping is programmed as 3 times at an ESD level, discharge is done 3 times.

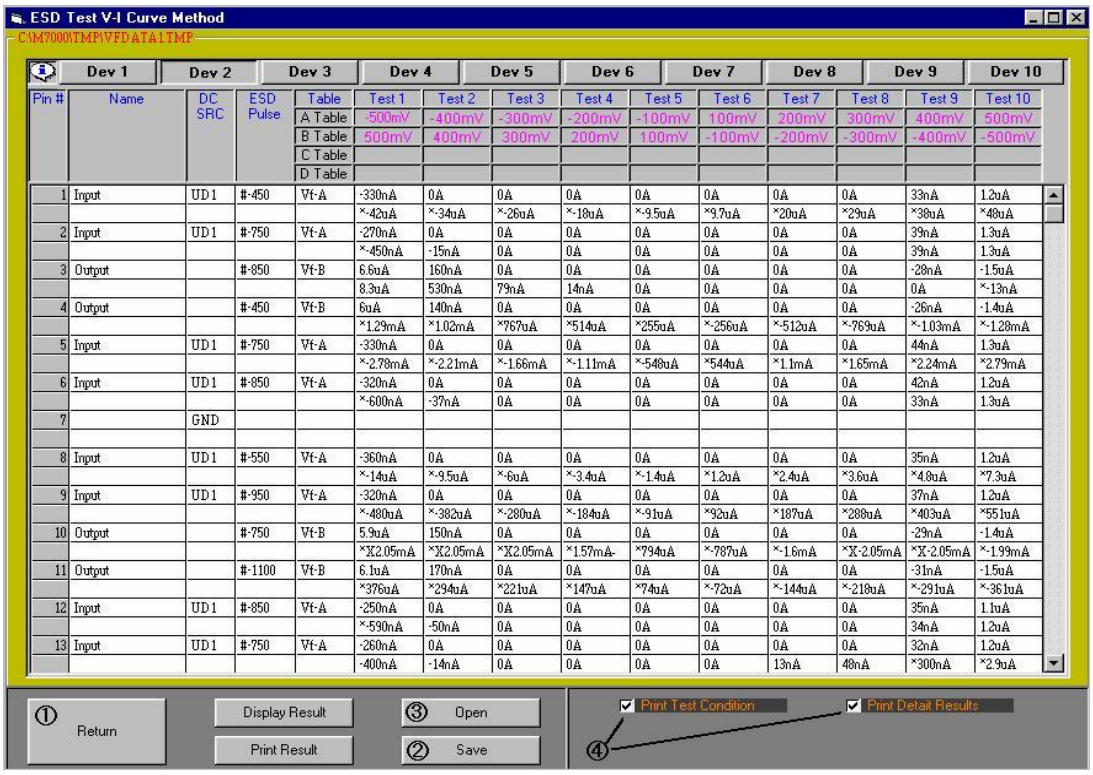
4.6 Breakage detection as well as degradation process measurement

Percent method of DC measurement enables device breakage by ESD stress.

Category method of DC measurement enables degradation process of the DUT by ESD stress.

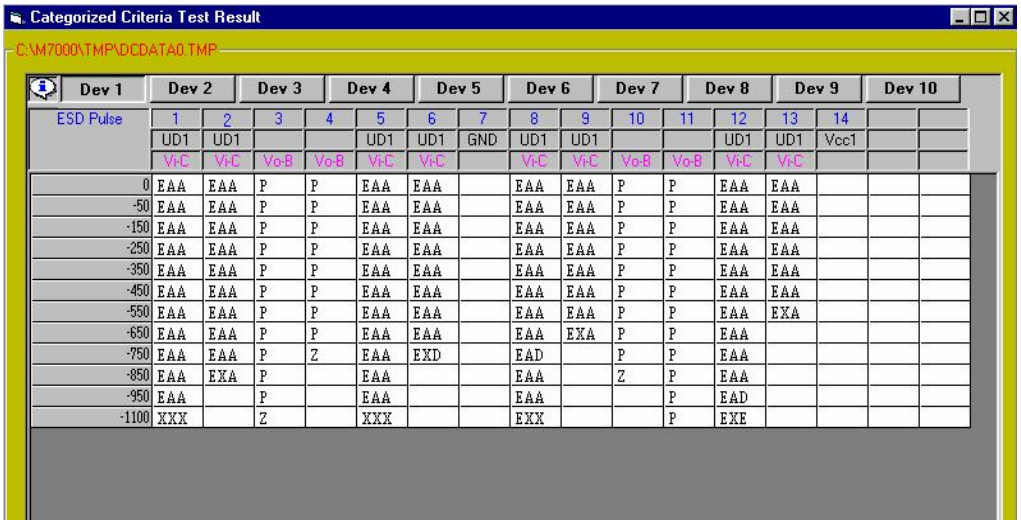
A Test result example of percent method

Next Table is an example of print out result. Upper rows are the currents before any zap, and lower rows are the currents at breakage. Breakage is detected by the percentage current change from the current before zap.



B. Test result example of M/M(Min/Max category) method

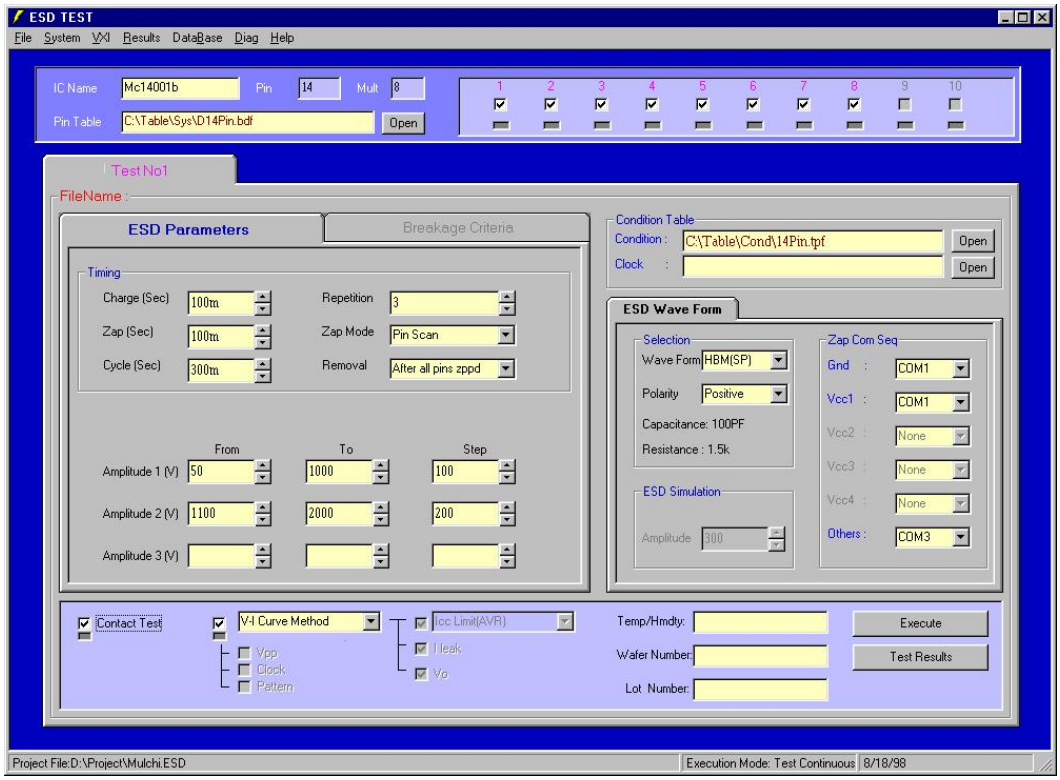
The table on next page is a test result example of M/M method. From the initial data(before zap) to degrade and breakage process can be listed.



4.7 Test conditions are easily made on the Windows 2000 OS

Following figure is an example menu to enter the test conditions of the percent(%) method. 2 or 3 sub-menu complete the programming. Once test is started, test process can be monitored by the display such as zap voltage, pin#, measured value, breakage decision, etc.

Printer, hard disk or floppy disk will save the program and/or test results by operator's request. Connection to the communication line is available.



4.8 Plentiful Tests

To meet every need of ESD test in semiconductor market, Model 7000 includes following tests that can be used with multiple device DUT board. High speed zapping is also available for all tests.

	Test Mode	Description
1	ESD simulation	Only zapping performed
2	V/I curve measurement	V/I curves of the DUT are measured
3*	DC measurement	DC parameter of the DUT are measured
4	ESD Test by % method	Combination of 1 and 2. Breakage is detected by the current change percentage.
5*	ESD Test by M/M method	Combination of 1 and 3. Degradation and breakage are detected by the DC parameter change.
6*	ESD Test by curve tracer	1 and external curve tracer is used. Operator decide DUT breakage by curve change.
7	Contact Test	Perform DUT contact test.
8	Self Test	System diagnostics

5. Latch-up Test (Model 7000EL, L type)

5.1 General

To get a repeatable test results of latch-up test, following 3 items are important.

- Stable trigger source
- Low impedance latch-up detection power supply
- Stabilize DUT

The Model 7000EL or L are designed in considering all above. The system also look at future upgrade of the relating standards.

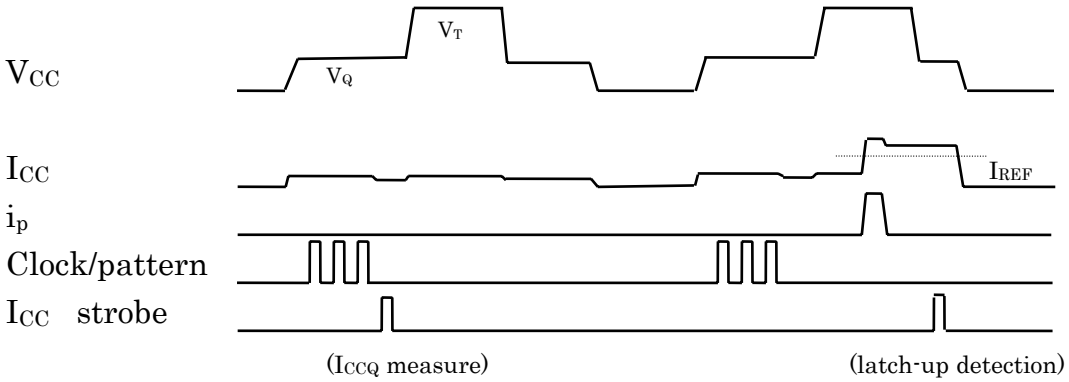
5.2 **Features**

- Meets EIAJ, JEDEC and ESD standard
- Plentiful latch-up trigger source
- Low impedance path and matrix by high current relay
- DUT stabilization by pull-up/down and clock/pattern generator
- Latch-up process measurement
- Detects temperature dependence
- Connection with emission microscope
- Plentiful test program
- Successive approximation high speed test

5.3 **Basic timing of latch-up test**

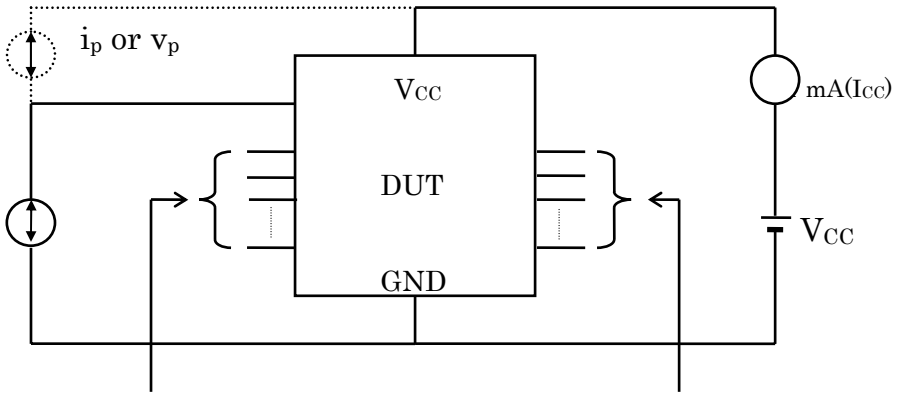
Next figure illustrates the test timing of current pulse triggered latch-up test.

- I_{CCQ}(quiescent I_{CC}) is measured after V_Q is applied to the DUT supply pins. I_{CCQ} may be measured after clock and/or pattern are applied to stabilize the DUT, as the figure below.
- Then i_p is applied to the test pin of the DUT. I_{CC} is measured after the programmed delay time. If measured I_{CC} exceeds I_{REF}(=I_{CCQ} x N + offset value), latch-up is detected and V_{CC} is forced to 0V.



5.4 **Latch-up test circuit**

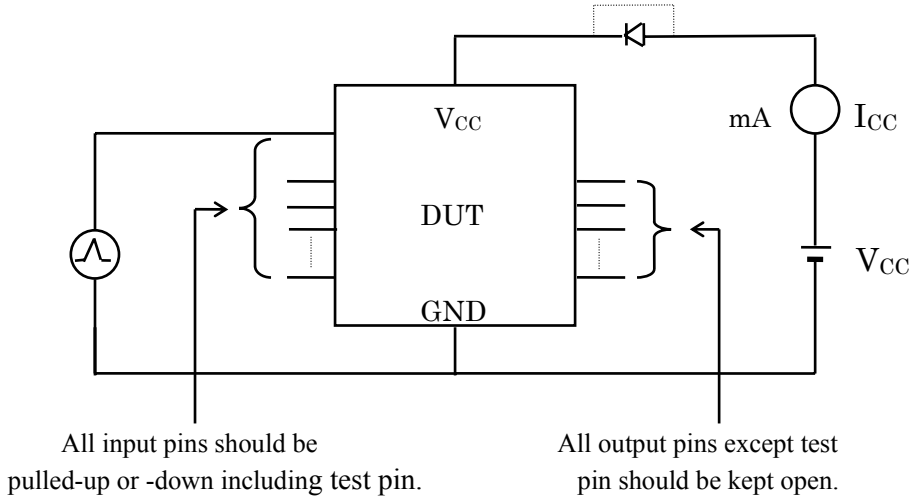
- Current pulse(i_p) or voltage pulse(v_p) triggered latch-up test



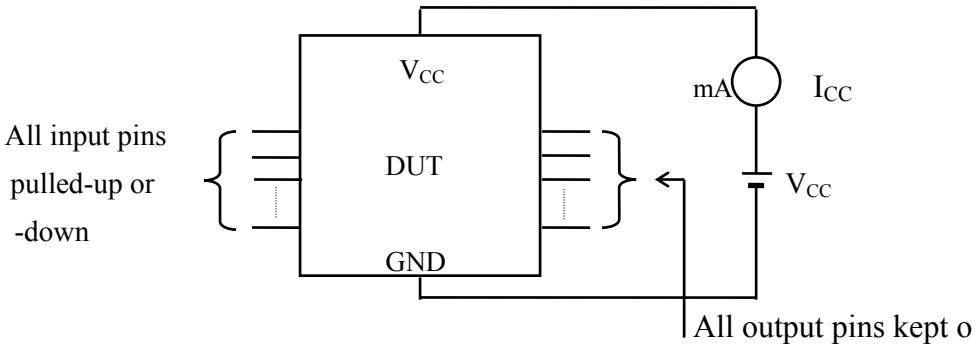
Input pins should be pulled up or down except test pin.

Output pins should be kept open except test pin.

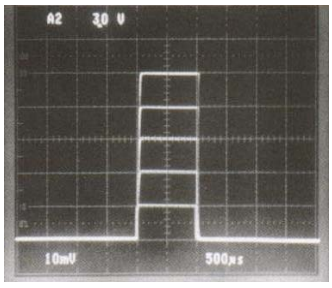
- **ESD or transient triggered latch-up test**



- Power supply pulse(V_P) triggered latch-up test

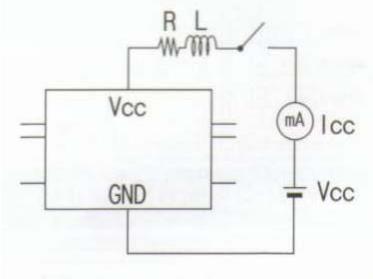


5.5 **Clean Current Pulse**



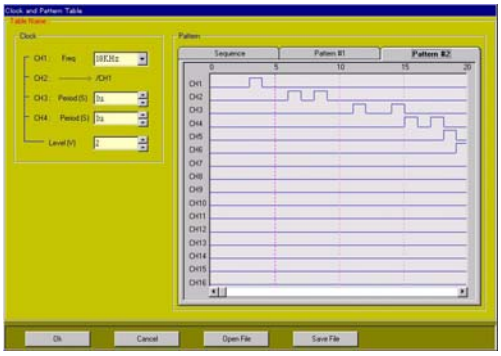
Latch-up repeatability depends on clean trigger source. The current pulse of Model 7000 has less than 5% distortion(overshoot and undershoot) as left picture. Variable t_r/t_f may be ordered as an option. After the trailing edge of the current pulse, input pin is pulled -up or -down without discontinuity, then I_{CC} is measured.

5.6 **Low power supply bus impedance**



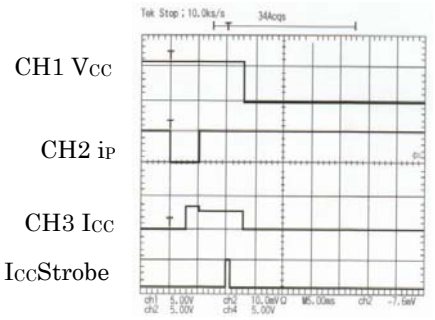
Because latch-up current is usually very high, voltage drop of the supply path causes recovery from latch-up, though once latched-up. This is a source of unstable measurement. To avoid it, Model 7000 uses low contact resistance and high current relay to switch V_{CC} supplies and decreases the impedance of supply path.

5.7 DUT stabilization



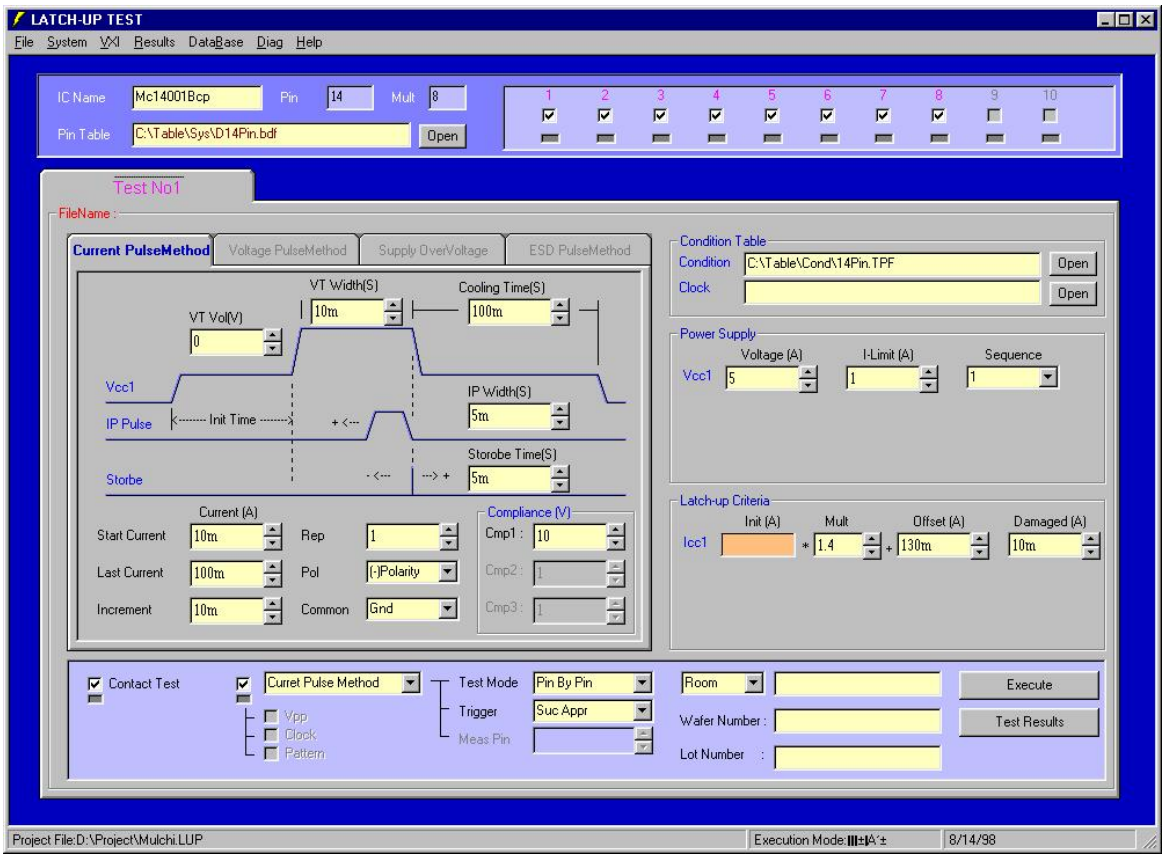
This window is to edit digital patterns to stabilize a DUT for ESD and latch-up test. Clocks and patterns are programmed by host PC windows. Higher density DUT needs some digital patterns before I_{CC} measurement.

5.8 To monitor latch-up process



The analysis of latch-up process has been difficult because the usual tester gives only digital results. Digitizing scope option stores the latch-up process and waveform information is easily collected as this picture. A-D converter board of PC may take over the scope, though bandwidth is limited. With the optional high temperature oven and emission microscope, further analysis such as temperature coefficient or latch-up location detection are possible.

5.9 Test conditions are easily made on the Windows 2000 OS



This window and a few sub-windows enable to decide latch-up test conditions and test execution. Up to 10 DUTs are automatically tested. Left window accepts i_p parameters such as timings, current, etc., V_{CC} voltage, sequence, latch-up definition. Pull-up, down, clock and pattern for DUT stabilization are programmed on the sub-windows. Input pins connected to clock or pattern are fixed to the level defined by the condition table during I_{CC} measurement.

5.10 Plentiful test modes

	Test mode	test pin
1	Current pulse triggered, incremental	I, O, I/O
2	Current pulse triggered, successive approximation	I, O, I/O
3*	Voltage pulse triggered, incremental	I, O, I/O
4*	Voltage pulse triggered, successive approximation	I, O, I/O
5*	ESD pulse triggered, incremental	I, O, I/O,V_{CC}
6*	ESD pulse triggered, successive approximation	I, O, I/O,V_{CC}
7	Supply pulse triggered, incremental	V_{CC}
8*	Transient pulse triggered, incremental	I, O, I/O,V_{CC}
9*	Transient pulse triggered, successive approx.	I, O, I/O,V_{CC}
10*	Punch through current measurement	I, I/O
11*	Temperature coefficient test	
12*	Test with emission microscope	
13	DUT contact test	
14	Self test, Diagnostics	

I : Input pin O : Output pin I/O : Input/Output pin

V_{CC} : Power Supply Pin GND : Ground pin

* : Optional

6. System Configuration

Type E : ESD test

Type EL : Both ESD and Latch-up test

Type L : Latch-up test

6.1 Pin count : 256/512/ 1024 pins

6.2 ESD section

	Function		E	EL	L
Type E/EL Auto Zap Auto Pin selection	High Voltage	1kV	Δ	Δ	NA
		4.5kV	◎	◎	NA
		8kV	Δ	Δ	NA
	Common pin relay matrix		◎	◎	NA
	EPG unit	HBM	◎	◎	NA
		MM	◎	◎	NA
		Others	Δ	Δ	NA
Type E/EL Auto Zap Auto pin sel.	X,Y axis robot		◎	◎	NA
	DUT board Loader/unloader	256 pins	Δ	Δ	NA
		512/1024 pins	◎	◎	NA
Type L Auto Zap Manual sel.	High voltage 1kV		NA	NA	◎
	MPG unit	MM	NA	NA	◎
		Others	NA	NA	Δ

6.3 DC section

Functions	E	EL	L
VF/IM	◎	◎	◎
$V_{CC}(V_P)$	Δ	◎	◎
V_{CC2}~V_{CC4}	Δ	Δ	Δ
DVM	Δ	◎	Δ
i_p	NA	◎	◎
v_p	NA	Δ	Δ
VF/IM self test board	◎	◎	◎

6.4 Stabilization section

Functions	E	EL	L
V_{CTL}(6 channels control power supply)	Δ	Δ	Δ
4 channels clock	Δ	Δ	Δ
16 channels pattern	Δ	Δ	Δ
256 channels pattern	Δ	Δ	Δ
Pull-up/down	Δ	◎	◎

6.5 Other functions

Functions	E	EL	L
High temperature oven and jig	NA	Δ	Δ
Scope to monitor ESD waveform and latch-up	Δ	Δ	Δ
Connection with emission microscope	NA	Δ	Δ
DUT board (IC socket supplied by the customer)	NA	Δ	Δ

◎ : Standard Δ : Optional NA : Not available